Instruction Manual

Tektronix

TMS 106
i386EX Microprocessor Support

070-9809-01

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

The common terminal is at ground potential. Do not connect the common terminal to elevated voltages.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Use Proper AC Adapter. Use only the AC adapter specified for this product.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 106 i386EX microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS 106 i386EX support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor support packages is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to supports on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data
- The TMS 106 i386EX probe adapter

Manual Conventions

This manual uses the following conventions:

- A number sign (#) following a signal name indicates an active low signal.
- The term “disassembler” refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of microprocessor support user manual.
- In the information on basic operations, the term “XXX” or “P54C” used in field selections and file names can be replaced with 386EX. This is the name of the microprocessor in field selections and file names you must use to operate the i386EX support.

- The term “SUT” (system under test) refers to the microprocessor-based system from which data will be acquired.
- The term “logic analyzer” refers to the Tektronix logic analyzer for which this product was purchased.
- The term “module” refers to a 102/136-channel, 96-channel module.
- 386EX refers to all supported variations of the i386EX microprocessor unless otherwise noted.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The user manual provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter contains information on the TMS 106 microprocessor support, and information on connecting your logic analyzer to your system under test.

Support Description

The TMS 106 microprocessor support disassembles data from systems that are based on the i386EX microprocessor. The support runs on a compatible Tektronix logic analyzer equipped with a 102/136-channel module, or a 96-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 106 microprocessor support.

The probe adapter accommodates the i386EX in a 132-pin PQFP package.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the *i386EX Microprocessor User's Manual,* Intel, 1994.

Information on basic operations also contains a general description of supports.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the i386EX support, the Tektronix logic analyzer must be equipped with at least a 102/136-channel module and a 96-channel module. The module must be equipped with enough probes to acquire channel and clock data from signals in your i386EX-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other i386EX support requirements and restrictions.

System Clock Rate. The microprocessor support product supports the i386EX microprocessor at speeds of up to 25 MHz. This specification is valid at the time this manual was printed. Please contact your Tektronix Sales Representative for current information on the fastest devices supported.

SUT Power. Whenever the SUT is powered off, be sure to remove power from the probe adapter. Refer to *Applying and Removing Power* at the end of this chapter for information on how to remove power from the probe adapter.

Configuring the Probe Adapter

There are seven jumpers on the probe adapter. One of them is the power source jumper, and the others are signal enabling jumpers.

Signal Enabling Jumpers

Some i386EX output pins can have multiple meanings depending on the reset configuration of the microprocessor. To ensure proper clocking and disassembly, jumpers J225, J230, J322, J325, and J330 must be configured to match the reset configuration of the microprocessor in the SUT. Refer to Table 1–1 for their jumper positions.

Table 1–1: Signal enabling jumpers

Jumper name	Description	Jumper pin position	386EX pin	Configured at reset as signal
J225	DACK0# Signal Enable	1–2	128	CS5#
		2–3		DACK0#
J230	HLDA Signal Enable	1–2	111	P1.7
		2–3		HLDA
J320	POWERDWN Signal Enable	1–2	86	P3.6
		2–3		POWERDWN

Table 1–1: Signal enabling jumpers (cont.)

Jumper name	Description	Jumper pin position	386EX pin	Configured at reset as signal
J322	REFRESH# Signal Enable	1–2	2	CS6#
		2–3		REFRESH#
J325	DACK1# Signal Enable	1–2	112	TXD1
		2–3		DACK1#
J330	LOCK# Signal Enable	1–2	107	P1.5
		2–3		LOCK#

Figure 1–1 shows the jumper locations of J225, J230, J320, J322, J325, J330, and the power source jumper J340 on the probe adapter.

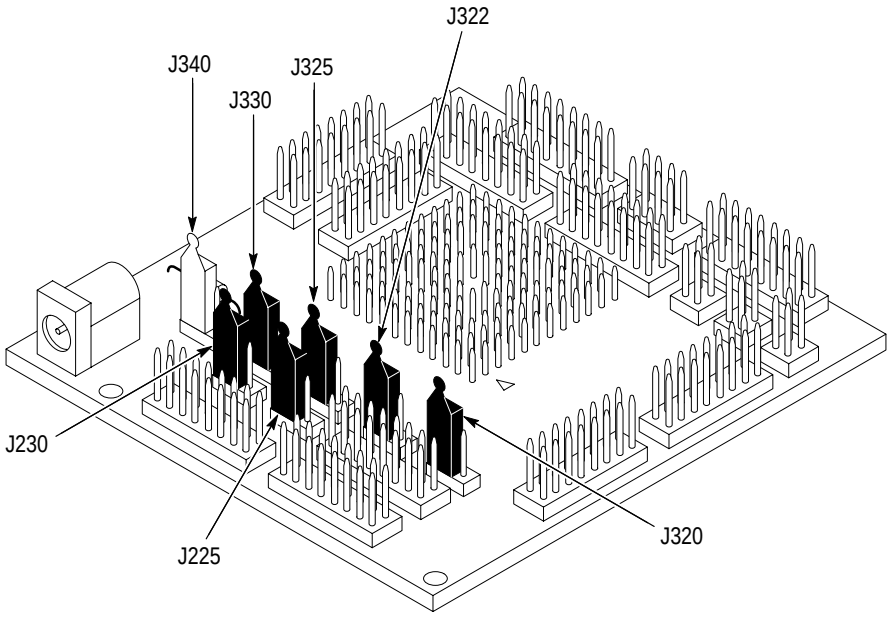


Figure 1–1: Signal enabling jumpers on the probe adapter

Power Source Jumper

Power source jumper J340 should be positioned on pins 2 and 3 if you have a +5 V i386EX and the probe adapter will be powered from the SUT.

If the probe adapter will be powered by an external source, position this jumper on pins 1 and 2.

For more information on using an alternate power source, refer to *Applying and Removing Power* on page 1–8.

Figure 1–2 shows the jumper location of J340 on the probe adapter.

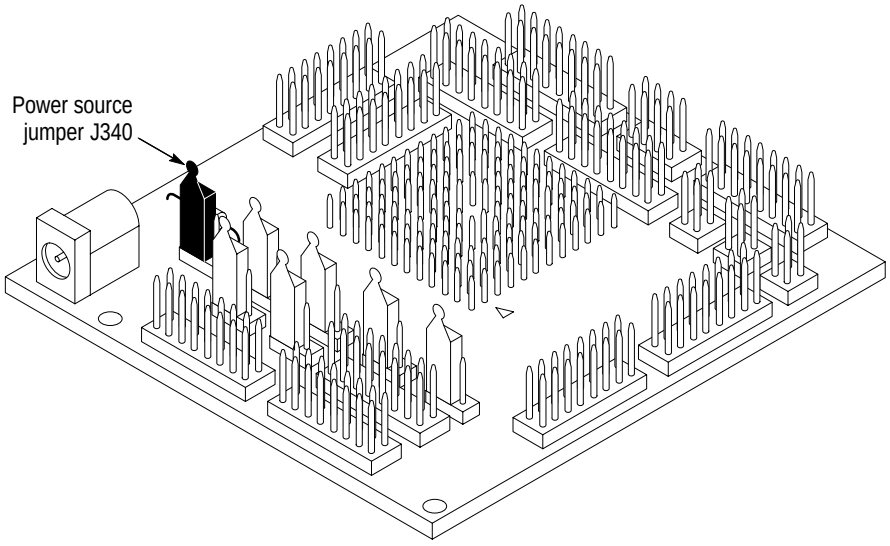


Figure 1–2: Power source jumper on the probe adapter

Connecting to a System Under Test

Before you connect to the SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the microprocessor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The channel and clock probes shown in this chapter are for a 102/136-channel module. Your probes will look different if you are using a 96-channel module.

The general requirements and restrictions of microprocessor supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

With a PQFP Probe Adapter

To connect the logic analyzer to a SUT using a PQFP probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
3. Place the probe adapter onto the antistatic shipping foam to support the probe as shown Figure 1–3. This prevents the circuit board from flexing.

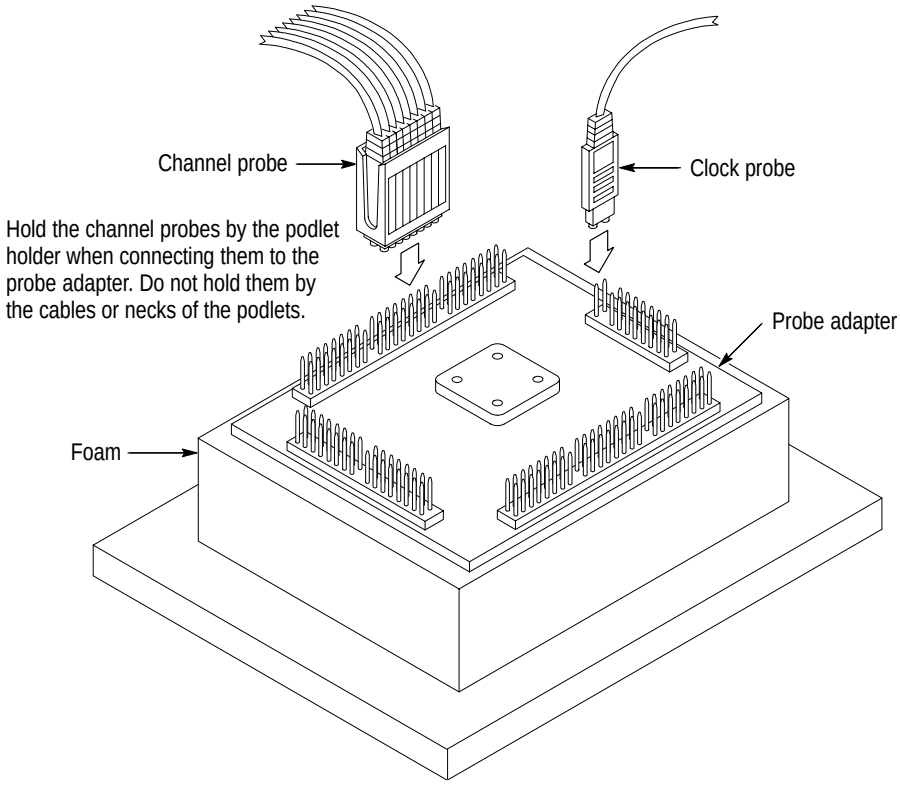


Figure 1–3: Connecting probes to a PQFP probe adapter

4. Connect the channel and clock probes to the probe adapter as shown in Figure 1–3. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

CAUTION. *This JEDEC PQFP (Plastic Quad Flat Pack) probe adapter has been equipped with a clip that has been designed for tight tolerances.*

The clip supports only Plastic Quad Flat Pack devices that conform to the JEDEC M0-069 October 1990 specification. Attaching the clip to a device that does not conform to this JEDEC standard can easily damage the clip's connection pins and/or the microprocessor, causing the probe adapter to malfunction.

Please contact your IC manufacturer to verify that the microprocessor you are targeting conforms to the JEDEC specification.

5. Remove the probe adapter from the shipping foam and carefully seat the PQFP test clip on the PGA socket pins on the underside of the probe adapter as shown in Figure 1–4 or Figure 1–5.

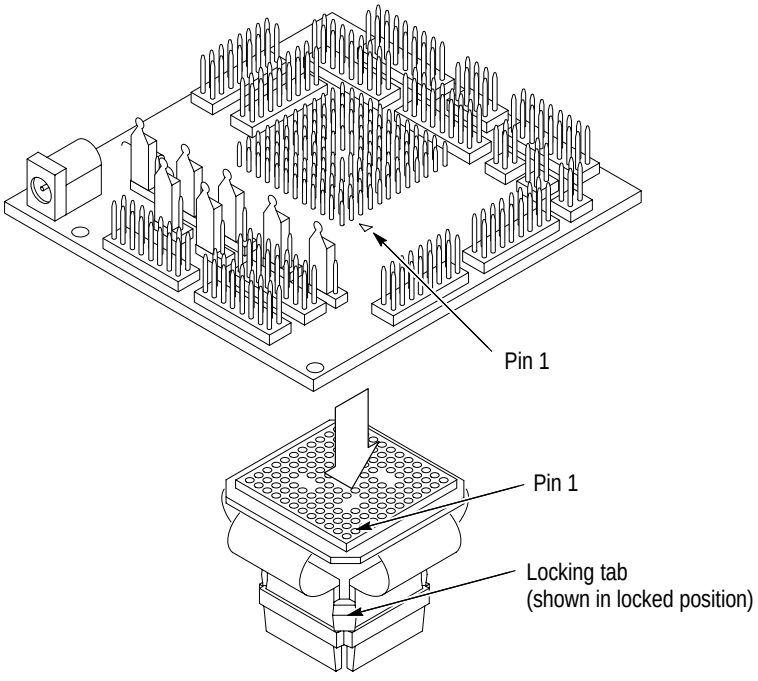


Figure 1–4: Connecting the test clip to the probe adapter

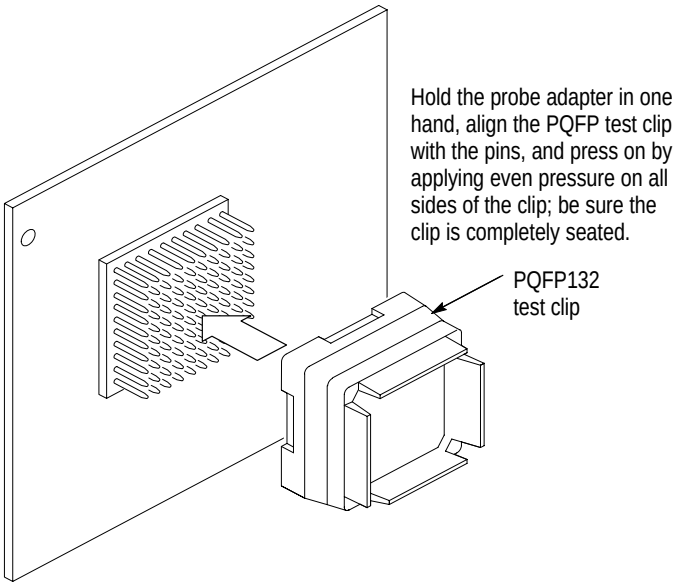


Figure 1–5: Connecting the older style test clip to the probe adapter

6. Line up the pin 1 indicator on the probe adapter circuit board (a white triangle) with the pin 1 indicator on the microprocessor.

CAUTION. *Failure to correctly place the probe adapter onto the microprocessor might permanently damage all electrical components when power is applied.*

Center the clip on the microprocessor and apply an equal downward force on all four sides of the clip, slightly rocking the probe adapter in a clockwise circle.

Do not apply leverage to the probe adapter when installing or removing it.

7. Verify that the test clip is not in the locked position by gently pulling on the test clip, or verifying that the locking tabs are in the upper position. Refer to Figure 1–4.

8. Place the probe adapter onto the SUT as shown in Figure 1–6.

9. Press on the probe adapter until the test clip locks onto the microprocessor.

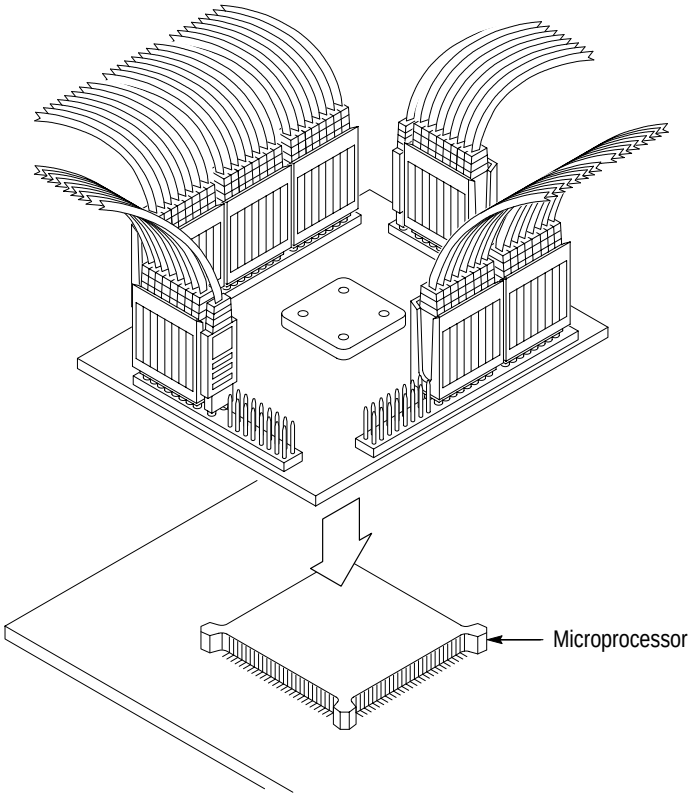


Figure 1–6: Placing a PQFP probe adapter onto the SUT

NOTE. *The probe adapter board might slip off or slip to one side of the microprocessor because of the extra weight of the probes. This can damage the microprocessor and the SUT. To prevent this from occurring, stabilize the probe adapter by placing a non-conductive object (such as foam) between the probe adapter and the SUT.*

Removing The Probe Adapter

To remove the probe adapter from the microprocessor on the SUT, gently but firmly pull up on the probe adapter. The test clip locking device will unlock and disengage.

Applying and Removing Power

If your microprocessor system cannot supply power to the i386EX probe adapter or your system has a +3.3 V i386EX microprocessor (probe adapters need +5 V), you must use an alternate power source. A +5 V power supply for the i386EX

probe adapter is available as an optional accessory. Refer to the *Replaceable Mechanical Parts* chapter for information on how to order a power supply.

The alternate power supply provides +5 volts to the i386EX probe adapter. The center connector of the power jack connects to Vcc.

***NOTE**. Whenever the SUT is powered off, be sure to remove power from the probe adapter.*

To apply power to the i386EX probe adapter and SUT, follow these steps:

***CAUTION.** Failure to use the +5 V power supply provided by Tektronix might permanently damage the probe adapter and i386EX microprocessor. Do not mistake another power supply that looks similar for the +5 V power supply.*

1. Connect the +5 V power supply to the jack on the probe adapter. Figure 1–7 shows the location of the jack on the adapter board.

***CAUTION.** Failure to apply power to the probe adapter before applying power to your SUT might permanently damage the i386EX microprocessor and SUT.*

2. Plug the power supply for the probe adapter into an electrical outlet.
3. Power on the SUT.

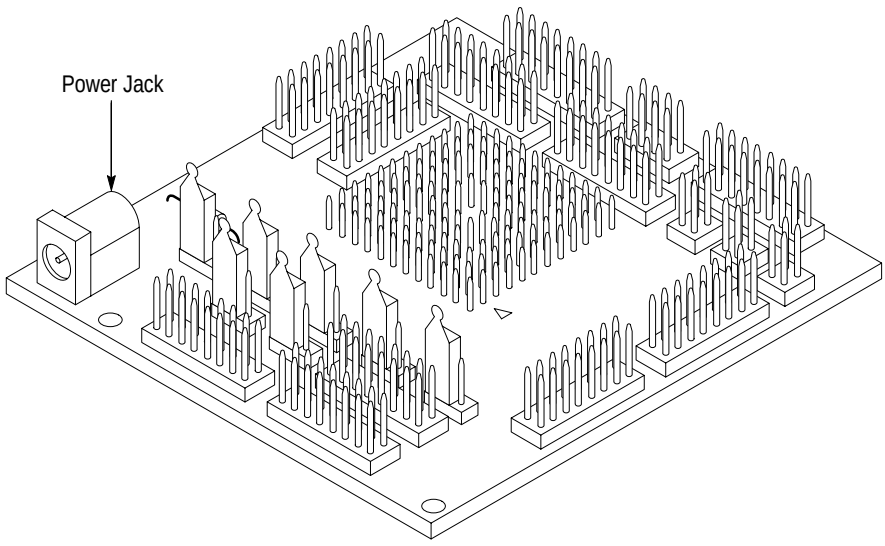


Figure 1–7: Location of the Power Jack

To remove power from the SUT and i386EX probe adapter, follow these steps:

CAUTION. *Failure to power down your SUT before removing the power from the probe adapter might permanently damage the i386EX microprocessor and SUT.*

1. Power down the SUT.
2. Unplug the power supply for the probe adapter from the electrical outlet.

Operating Basics

Setting Up the Support

The information in this section is specific to the operations and functions of the TMS 106 i386EX support on any Tektronix logic analyzer for which it can be purchased.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the i386EX support are Address, Data, Control, Intr, Copr, ChipSel, and Misc. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 3–6.

Clocking Options

The TMS 106 support offers a microprocessor-specific clocking mode for the i386EX microprocessor. This clocking mode is the default selection whenever you select the 386EX support.

A description of how cycles are sampled by the module using the support and probe adapter is found in the *Specifications* chapter.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

The clocking option for the TMS 106 support is DMA Cycles.

DMA Cycles A DMA cycle is defined as the i386EX microprocessor giving up the bus to an alternate device (a DMA device or another microprocessor). These types of cycles are acquired when you select Included.

Symbols

The TMS 106 support supplies one symbol table file. The 386EX_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file, 386EX_Ctrl in the Control channel group symbol table.

Information on basic operations describes how to use symbolic values for triggering, and displaying other channel groups symbolically, such as the Address channel group.

Table 2–1: Control group symbol table definitions

Symbol	Control group value LBA# BS8_L# DACK1# DACK0# SMIACT# REFRESH# RESET_L BHE# HLDA READY# LOCK# M/IO# D/C# W/R#	Meaning
RVP_LCK_R	X X 1 1 1 1 0 X 0 0 0 1 1 0	Locked read to R,V, or P space
SMM_LCK_R	X X 1 1 0 1 0 X 0 0 0 1 1 0	Locked read to SMM space
LOCKED_RD*	X X 1 1 X 1 0 X 0 0 0 1 1 0	Any Locked read
RVP_LCK_W	X X 1 1 1 1 0 X 0 0 0 1 1 1	Locked write to R,V, or P space
SMM_LCK_W	X X 1 1 0 1 0 X 0 0 0 1 1 1	Locked write to SMM space
LOCKED_WR*	X X 1 1 X 1 0 X 0 0 0 1 1 1	Any Locked write
RVP_FETCH	X X 1 1 1 1 0 X 0 0 X 1 0 0	Fetch from R, V, or P space
SMM_FETCH	X X 1 1 0 1 0 X 0 0 X 1 0 0	Fetch from SMM space
FETCH*	X X 1 1 X 1 0 X 0 0 X 1 0 0	Any Fetch
RVP_MEM_R	X X 1 1 1 1 0 X 0 0 X 1 1 0	Memory read from R, V, or P space
SMM_MEM_R	X X 1 1 0 1 0 X 0 0 X 1 1 0	Memory read from SMM space
MEM_READ*	X X 1 1 X 1 0 X 0 0 X 1 1 0	Any Memory read
RVP_MEM_W	X X 1 1 1 1 0 X 0 0 X 1 1 1	Memory write to R, V, or P space
SMM_MEM_W	X X 1 1 0 1 0 X 0 0 X 1 1 1	Memory write to SMM space
MEM_WRITE*	X X 1 1 X 1 0 X 0 0 X 1 1 1	Any Memory write
RVP_IO_RD	X X 1 1 1 1 0 X 0 0 X 0 1 0	I/O read from R, V, or P space
SMM_IO_RD	X X 1 1 0 1 0 X 0 0 X 0 1 0	I/O read from SMM space
IO_READ*	X X 1 1 X 1 0 X 0 0 X 0 1 0	Any I/O read
RVP_IO_WR	X X 1 1 1 1 0 X 0 0 X 0 1 1	I/O write to R, V, or P space
SMM_IO_WR	X X 1 1 0 1 0 X 0 0 X 0 1 1	I/O write to SMM space
IO_WRITE*	X X 1 1 X 1 0 X 0 0 X 0 1 1	Any I/O write
RVP_MEM*	X X 1 1 1 1 0 X 0 0 X 1 1 X	Any Memory access in R,V,or P space

Table 2–1: Control group symbol table definitions (cont.)

Symbol	Control group value LBA# BS8_L# DACK1# DACK0# SMIACT# REFRESH# RESET_L BHE# HLDA READY# LOCK# M/IO# D/C# W/R#	Meaning
SMM_MEM*	X X 1 1 0 1 0 X 0 0 X 1 1 X	Any Memory access from/to SMM space
MEMORY*	X X 1 1 X 1 0 X 0 0 X 1 1 X	Any Memory access
RVP_IO*	X X 1 1 1 1 0 X 0 0 X 0 1 X	Any I/O access in R, V, or P space
SMM_IO*	X X 1 1 0 1 0 X 0 0 X 0 1 X	Any I/O read from/to SMM space
IO*	X X 1 1 X 1 0 X 0 0 X 0 1 X	Any I/O access
RVP_READ*	X X 1 1 1 1 0 X 0 0 X X 1 0	Any Read from R, V, or P space
SMM_READ*	X X 1 1 0 1 0 X 0 0 X X 1 0	Any Read from SMM space
READ*	X X 1 1 X 1 0 X 0 0 X X 1 0	Any Read
RVP_WRITE*	X X 1 1 1 1 0 X 0 0 X X 1 1	Any Write to R, V, or P space
SMM_WRITE*	X X 1 1 0 1 0 X 0 0 X X 1 1	Any Write to SMM space
WRITE*	X X 1 1 X 1 0 X 0 0 X X 1 1	Any Write
RVP_I_ACK	X X 1 1 1 1 0 X 0 0 X 0 0 0	Interrupt acknowledge in R, V, or P space
SMM_I_ACK	X X 1 1 0 1 0 X 0 0 X 0 0 0	Interrupt acknowledge in SMM space
INT_ACK*	X X 1 1 X 1 0 X 0 0 X 0 0 0	Any Interrupt acknowledge
HALT_SHUT	X X 1 1 X 1 0 X 0 0 X 1 0 1	Halt or Shutdown Cycle
RVP_LOCKD*	X X 1 1 1 1 0 X 0 0 0 X X X	Any Locked cycle in R,V,P space
SMM_LOCKD*	X X 1 1 0 1 0 X 0 0 0 X X X	Any Locked cycle in SMM space
LOCKED*	X X 1 1 X 1 0 X 0 0 0 X X X	Any Locked cycle
RVP_RSRVD	X X 1 1 1 1 0 X 0 0 X 0 0 1	Reserved cycle in R, V, or P space
SMM_RSRVD	X X 1 1 0 1 0 X 0 0 X 0 0 1	Reserved cycle in SMM space
RESERVED*	X X 1 1 X 1 0 X 0 0 X 0 0 1	Any Reserved cycle
REFRESH	X X X X X 0 0 X X X X X X X	DRAM Refresh cycle
DMA_CH1	X X 0 X X X 0 X X X X X X X	DMA access on Channel 1
DMA_CH0	X X X 0 X X 0 X X X X X X X	DMA access on Channel 0
DMA	X X X X X X 0 X 1 X X X X X	DMA access using HLDA
RVP_HI_XR	X X X X 1 1 0 0 X X X X X X	Hi bit transfer in R, V, or P space
SMM_HI_XR	X X X X 0 1 0 0 X X X X X X	Hi bit transfer in SMM space
HIGH_XFER*	X X X X X 1 0 0 X X X X X X	Any Hi bit transfer
RESET	X X X X X X 1 X X X X X X X	Processor Reset
RVP*	X X X X 1 X 0 X X X X X X X	Any access in R, V, or P space
SMM*	X X X X 0 X 0 X X X X X X X	Any access in SMM space

*** Symbols used only for triggering and are not displayed.**

Acquiring and Viewing Disassembled Data

This section describes how to acquire and view disassembled data.

Acquiring Data

Once you load the 386EX support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

You can view disassembled data in four different display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–9.*

The default display format shows the Address, Data, and Control channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–2 shows the special characters and strings displayed by the i386EX disassembler and gives a definition of what they represent.

Table 2–2: Special characters in the display and meaning

Character or string displayed	Meaning
>> on the TLA 700 m on the DAS 9200	The interpretation of the instruction was manually changed using the Mark Cycle function
#	Indicates an immediate value
t	Indicates the number shown is in decimal, such as #12t

Table 2–2: Special characters in the display and meaning (cont.)

Character or string displayed	Meaning
****	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks will indicate the width of the data that is unavailable. Two asterisks represent a byte.
(16) or (32)	Indicates if the default code segment size is 16 or 32 bits. This is for fetch cycles only.
SMM	Indicates a System Management Mode cycle.
* ILLEGAL INSTRUCTION *	Decoded as an illegal instruction

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–3 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2–3: Cycle type definitions

Cycle type	Definition
(MEM_READ)	A read from memory that is not an opcode fetch
(MEM_WRITE)	Any write to memory
(I/O_READ)	A read from an I/O port
(I/O_WRITE)	A write to an I/O port
(INT_ACK)	An interrupt acknowledge cycle
(LOCKED MEM READ)	A read from memory that is locked
(LOCKED MEM WRITE)	A write to memory that is locked
(DMA CYCLE)	A direct memory access cycle
(CO I/O READ)	A read access from an I/O port on the coprocessor
(CO I/O WRITE)	A write access to an I/O port on the coprocessor
(DMA CHANNEL 0)	A DMA access on channel 0
(DMA CHANNEL 1)	A DMA access on channel 1
(SHUTDOWN)	A shutdown cycle of type HALT/SHUTDOWN; address = 0H
(HALT)	A halt cycle of type HALT/SHUTDOWN; address = 02H
(RESERVED)	A reserved cycle
(RESET)	A reset cycle
(REFRESH)	A memory data read with REFRESH# asserted or a memory data read with BHE# and BLE# driven high

Table 2–3: Cycle type definitions (cont.)

Cycle type	Definition
(INVALID CYCLE)	A combination of control bits that is unexpected or unrecognized
(EXTENSION) §	A fetch cycle computed to be an opcode extension
(FLUSH) §	A fetch cycle computed to be an opcode flush

§ **Computed cycle types.**

Figure 2–1 shows an example of the Hardware display.

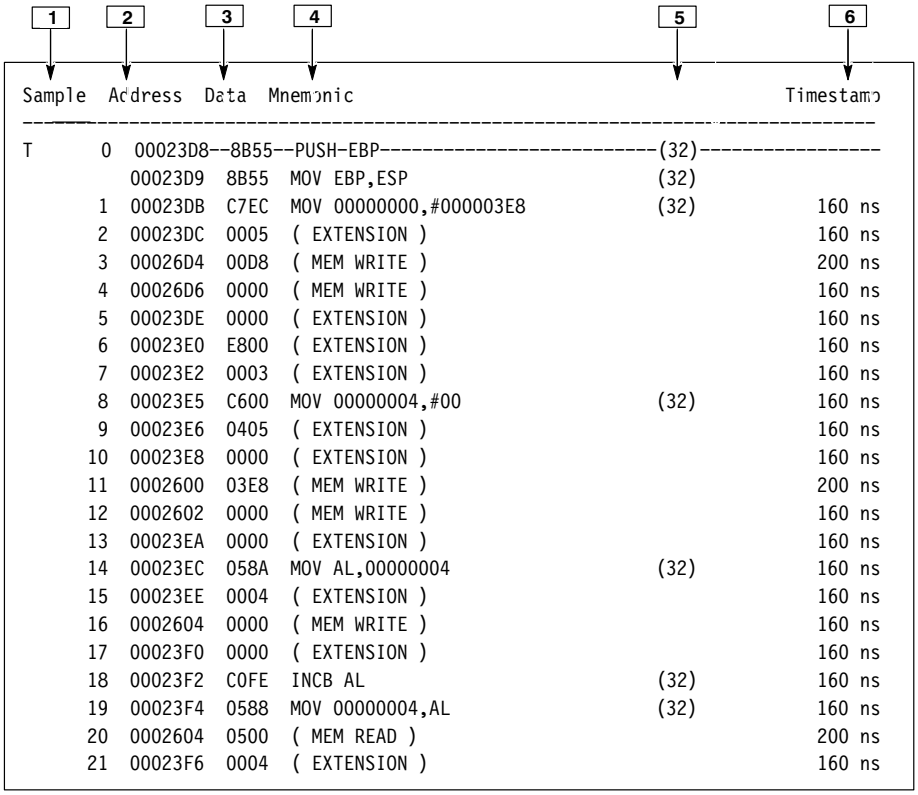


Figure 2–1: Hardware Display

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **Address Group.** Lists data from channels connected to the i386EX Address bus.

3 **Data Group.** Lists data from channels connected to the i386EX Data bus.

4 **Mnemonic Column.** Lists the disassembled instructions and cycle types.

5 This part of the mnemonic, (16) or (32), indicates that the fetch is from a 16- or 32-bit code segment size and disassembled accordingly.

6 **Timestamp.** Lists the timestamp values when a timestamp selection is made. Information on basic operations describes how you can select a timestamp.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions will be used to disassemble the instruction, but will not be displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

Instructions that generate a change in the flow of control in the i386EX are as follows:

BOUND	JBE/JNA	JNE/JNZ	JS
CALL	JCXZ/JECXZ	JNL/JGE	LOOP
DIV	JE/JZ	JNLE/JG	LOOPNZ/LOOPNE
IDIV	JL/JNGE	JNO	LOOPZ/LOOPE
INT	JLE/JNG	JNP/JPO	RET
INTO	JMP	JNS	RSM
IRET	JNB/JAE/JNC	JO	JB/JNAE/JC
JNBE/JA	JP/JPE		

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the i386EX are as follows:

BOUND	IDIV	IRET
CALL	INT	RET
DIV	INTO	RSM

Changing How Data is Displayed

There are fields and features that allow you to further modify displayed data to suit your needs. You can make selections unique to the i386EX support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

There are no optional fields for this support package. Refer to the information on basic operations for descriptions of common fields.

Optional Display Selections

You can make optional selections for disassembled data. In addition to the common selections that are described in the information on basic operations, you can change the displayed data in the following ways:

- Select code segment size
- Choose an interrupt table
- Specify the starting address of the interrupt table
- Specify the size of the interrupt table
- Specify whether to use BS8# and BHE# to dash invalid bytes

The i386EX support has four additional fields: Code Segment Size, Interrupt Table, Interrupt Table Address, and Invalid Bytes. These fields appear in the area indicated in the information on basic operations.

Code Segment Size. You can select the default code size: 32-bit or 16-bit. The default code size is 16-bit.

Interrupt Table. You can specify if the interrupt table is Real, Virtual, or Protected. (Selecting Virtual is equivalent to selecting Protected.) The default is Real.

Interrupt Table Address. You can specify the starting address of the interrupt table in hexadecimal. The default starting address is 0x0000000.

Interrupt Table Size. You can specify the size of the interrupt table in hexadecimal. The default size is 0x400.

Invalid Bytes (– –). You can specify whether to use lines BS8# and BHE# as a reliable bus size and byte selection indicator. If you select BS8#/BHE#, the

disassembly software will assume that these two signals are driven to their correct state for each cycle, and automatically display the invalid byte as dashes. Otherwise, by default, the disassembly software will display both the upper and lower bytes for 16-bit and 8-bit data transfers.

Figure 2–2 shows an example of when BS8#/BHE# is selected for the Invalid Bytes (––) field; Figure 2–3 shows an example of when Unchanged is selected.

Sample	Address	Data	Mnemonic		Timestamp
122	0002542	FF4D	(EXTENSION)		160 ns
123	0002544	F980	CMP CL,#07	(32)	160 ns
124	00026C7	01--	(MEM READ)		200 ns
125	0002547	0F07	JNBE 0002584	(32)	160 ns
126	00026C7	02--	(MEM WRITE)		160 ns
127	00026C7	02--	(MEM READ)		160 ns
128	0002548	3787	(EXTENSION)		160 ns
129	000254A	0000	(EXTENSION)		160 ns
130	000254D	0F00	MOVZXB EAX,08[EBP]	(32)	160 ns
131	000254E	45B6	(EXTENSION)		160 ns
132	0002551	D308	SAL EAX,CL	(32)	160 ns
133	0002553	88E0	MOV FE[EBP],AL	(32)	160 ns
134	0002554	FE45	(EXTENSION)		160 ns
135	00026D0	--01	(MEM READ)		200 ns
136	0002556	B60F	MOVZXB EAX,AL	(32)	160 ns
137	0002559	F7C0	TEST EAX,#00000080	(32)	160 ns
138	000255A	80C0	(EXTENSION)		160 ns
139	00026C6	--04	(MEM WRITE)		160 ns
140	000255C	0000	(EXTENSION)		160 ns
141	000255F	0F00	JE 0002574	(32)	160 ns
142	0002560	0F84	(EXTENSION)		160 ns
143	0002562	0000	(EXTENSION)		160 ns
144	0000293	----	(REFRESH)		200 ns

Figure 2–2: BS8#/BHE# Selected for Invalid Bytes (––)

Sample	Address	Data	Mnemonic		Timestamp
123	0002544	F980	CMP CL,#07	(32)	160 ns
124	00026C7	0180	(MEM READ)		200 ns
125	0002547	0F07	JNBE 0002584	(32)	160 ns
126	00026C7	0202	(MEM WRITE)		160 ns
127	00026C7	0202	(MEM READ)		160 ns
128	0002548	3787	(EXTENSION)		160 ns
129	000254A	0000	(EXTENSION)		160 ns
130	000254D	0F00	MOVZXB EAX,08[EBP]	(32)	160 ns
131	000254E	45B6	(EXTENSION)		160 ns
132	0002551	D308	SAL EAX,CL	(32)	160 ns
133	0002553	88E0	MOV FE[EBP],AL	(32)	160 ns
134	0002554	FE45	(EXTENSION)		160 ns
135	00026D0	FE01	(MEM READ)		200 ns
136	0002556	B60F	MOVZXB EAX,AL	(32)	160 ns
137	0002559	F7C0	TEST EAX,#00000080	(32)	160 ns
138	000255A	80C0	(EXTENSION)		160 ns
139	00026C6	0404	(MEM WRITE)		160 ns
140	000255C	0000	(EXTENSION)		160 ns
141	000255F	0F00	JE 0002574	(32)	160 ns
142	0002560	0F84	(EXTENSION)		160 ns
143	0002562	0000	(EXTENSION)		160 ns
144	0000293	----	(REFRESH)		200 ns
145	0002564	0F00	(EXTENSION)		280 ns

Figure 2–3: Unchanged Selected for Invalid Bytes (––)

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it to one of the following cycle types:

- Opcode (the first word of an instruction)
- Extension (a subsequent word of an instruction)
- Flush (an opcode or extension that is fetched, but not executed)
- Anything (any valid opcode, extension or flush)
- Read (marks a memory reference read as data)

Mark selections for 16-bit instruction fetch cycles:

Any	OPCODE
OPCODE	Any
Ext	Ext
Flush	Flush

16 Bit Default Segment Size
32 Bit Default Segment Size

Undo marks on this cycle

Mark selections for 8-bit instruction fetch cycles:

OPCODE
Ext
Flush

16 Bit Default Segment Size
32 Bit Default Segment Size

Undo marks on this cycle

You can also use the F4: Mark Cycle key to specify the default segment size mode (16-bit or 32-bit) for the cycle. The segment size selection changes the cycle the cursor is on and the remaining cycles to the end of memory or to the next mark.

The default segment size of the cycle is independent of any prefix override bytes in the particular fetch. For example, if you mark cycle 455 with a default size of 32 bits, but there are address/operand override prefixes in the instruction, the default size will be 32 bits, but the size of the instruction will be 16 bits.

Displaying Exception Vectors

The disassembler can display i386EX exception vectors. You can select to display the interrupt vectors for Real, Virtual, or Protected mode in the Interrupt Table field. (Selecting Virtual is equivalent to selecting Protected.)

You can relocate the table by entering the starting address in the Interrupt Table Address field. The Interrupt Table Address field provides the disassembler with the offset address; enter an eight-digit hexadecimal value corresponding to the offset of the base address of the exception table. The Interrupt Table Size field lets you specify a three-digit hexadecimal size for the table.

You can make these selections in the Disassembly property page (the Disassembly Format Definition overlay).

Information on basic operations tells you where you can make optional display selections for the acquisition module.

Table 2–4 lists the i386EX exception vectors for the Real Addressing mode.

Table 2–4: Interrupt vectors for real mode

Exception number	Location in IV † (in hexadecimal)	Displayed interrupt name
0	0000	DIVIDE ERROR
1	0004	DEBUG EXCEPTIONS
2	0008	NMI INTERRUPT
3	000C	BREAKPOINT INTERRUPT
4	0010	INTO DETECTED OVERFLOW
5	0014	BOUND RANGE EXCEEDED
6	0018	INVALID OPCODE
7	001C	COPROCESSOR NOT AVAILABLE
8	0020	INTERESTED TABLE LIMIT TOO SMALL
9-11	0024-002C	RESERVED
12	0030	STACK EXCEPTION
13	0034	SEGMENT OVERRUN
14-15	0038-003C	RESERVED
16	0040	COPROCESSOR MODE
17-31	0044-007C	RESERVED
32-255	0080-03FC	USER DEFINED

† **IV means interrupt vector table.**

Table 2–5 lists the i386EX exception vectors for the Protected Addressing mode.

Table 2–5: Interrupt vectors for protected mode

Exception number	Location in IDT † (in hexadecimal)	Displayed interrupt name
0	0000	DIVIDE ERROR
1	0008	DEBUG EXCEPTIONS
2	0010	NMI INTERRUPT
3	0018	BREAKPOINT INTERRUPT
4	0020	INTO DETECTED OVERFLOW
5	0028	BOUND RANGE EXCEEDED
6	0030	INVALID OPCODE
7	0038	DEVICE NOT AVAILABLE
8	0040	DOUBLE FAULT
9	0048	RESERVED
10	0050	INVALID TSS
11	0058	SEGMENT NOT PRESENT
12	0060	STACK EXCEPTION
13	0068	GENERAL PROTECTION
14	0070	PAGE FAULT
15	0078	RESERVED
16	0080	COPROCESSOR MODE
17	0088	ALIGNMENT CHECK
18-31	0090-00F8	RESERVED
32-255	0100-07F8	USER DEFINED

† **IDT means interrupt descriptor table.**

Specifications

Specifications

This chapter contains information on the specifications of the probe adapter as well as:

- Channel assignment tables
- Description of how the module acquires i386EX signals
- List of other accessible i386EX signals and extra acquisition channels

Probe Adapter Description

The probe adapter is a nonintrusive piece of hardware that allows the acquisition module to acquire data from a i386EX microprocessor in its own operating environment with little affect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for a i386EX microprocessor. The probe adapter connects to the microprocessor in the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

Circuitry on the probe adapter can be powered from either the SUT or an external power source. Refer to *Applying and Removing Power* in the *Getting Started* section for information on using an external power source.

The probe adapter accommodates the i386EX in a 132-pin PQFP package.

Configuration

There are seven jumpers on the probe adapter. One of them is the power source jumper and the others are signal enabling jumpers.

Signal Enabling Jumpers. Some i386EX output pins can have multiple meanings depending on the reset configuration of the microprocessor. To ensure proper clocking and disassembly, jumpers J225, J230, J322, J325, and J330 must be configured to match the reset configuration of the microprocessor in the SUT. Refer to Table 3–1 for their jumper positions.

Table 3–1: Signal enabling jumpers

Jumper name	Description	Jumper pin position	386EX pin	Configured at reset as signal
J225	DACK0# Signal Enable	1–2	128	CS5#
		2–3		DACK0#
J230	HLDA Signal Enable	1–2	111	P1.7
		2–3		HLDA
J320	POWERDWN Signal Enable	1–2	86	P3.6
		2–3		POWERDWN
J322	REFRESH# Signal Enable	1–2	2	CS6#
		2–3		REFRESH#
J325	DACK1# Signal Enable	1–2	112	TXD1
		2–3		DACK1#
J330	LOCK# Signal Enable	1–2	107	P1.5
		2–3		LOCK#

Figure 3–1 shows the jumper locations of J225, J230, J320, J322, J325, J330, and power jumper J340 on the probe adapter.

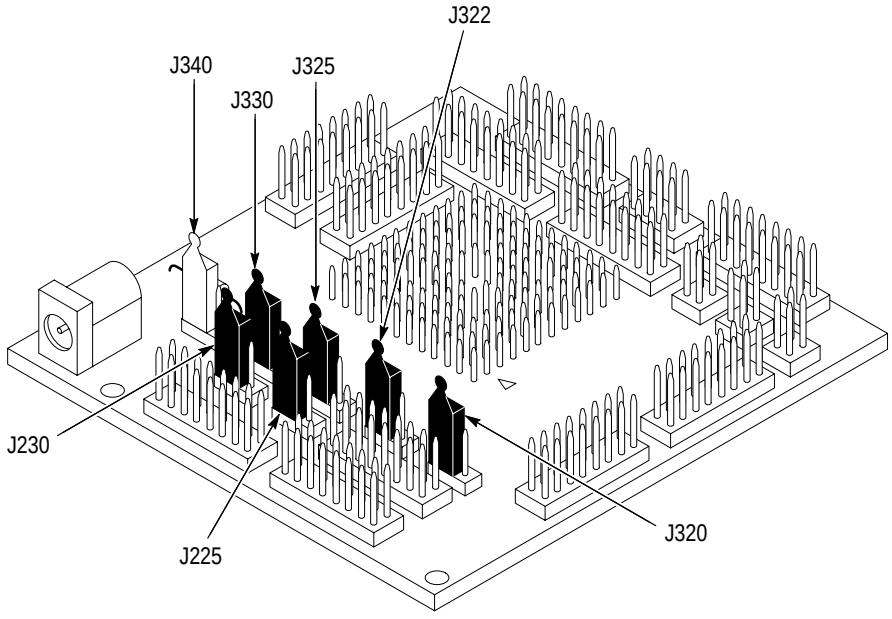


Figure 3–1: Jumpers on the probe adapter

Power Source Jumper. Power Source jumper J340 should be positioned on pins 2 and 3 if you have a +5 V i386EX and the probe adapter will be powered from the SUT.

If the probe adapter will be powered by an external source, position this jumper on pins 1 and 2.

Specifications

In Table 3–2, for the 102/136-channel module, one podlet load is 20 kΩ in parallel with 2 pF. For the 96-channel module, one podlet load is 100 kΩ in parallel with 10 pF. Table 3–3 lists the environmental specifications. Table 3–4 lists the certifications and compliances that apply to the probe adapter. Figure 3–2 shows the dimensions of the PLCC probe adapter.

Table 3–2: Electrical specifications

Characteristics	Requirements	
SUT DC Power Requirements		
Voltage	4.75-5.25 VDC	
Current	I max (calculated) 420 mA I typ (measured) 310 mA	
SUT Clock		
Clock Rate	Min. DC Max. 25 MHz	
Minimum Setup Time Required		
All Signals	5 ns	
Minimum Hold Time Required		
All Signals	0 ns	
	Specification	
Measured Typical SUT Signal Loading	**AC Load[1]**	**DC Load**
CLK2	16 pF	20R6–5
RESET	25 pF	22V10–10 in parallel with 20R6–5
NA#, BS8#	18 pF + 1 podlet	1 podlet in parallel with 20R6–5
READY#, ADS#	12 pF + 1 podlet	1 podlet in parallel with 22V10–10
PEREQ, ERROR#, BUSY#, DRQ0, DRQ1, SMIACT#, HOLD, UCS#, LBA#, RD#, W/R#, M/IO#, WR#, D/C#, NMI A31:1, BHE#, BLE#	6 pF + 1 podlet	1 podlet
D15:0, CS6:0	8–12 pF + 1 podlet	1 podlet
386EX Pin		

Table 3–2: Electrical specifications (cont.)

Characteristics	Requirements	
128 = CS5# (J225 in 1–2 position)	6 pF + 1 podlet	1 podlet
128 = DACK0# (J225 in 2–3 position)	26 pF + 2 podlets	2 podlets in parallel with 20R6–5
111 = P1.7 (J230 in 1–2 position)	6 pF	
111 = HLDA (J230 in 2–3 position)	20 pF + 1 podlet	1 podlet in parallel with 20R6–5
86 = P3.6 (J320 in 1–2 position)	6 pF	
86 = POWERDWN (J320 in 2–3 position)	20 pF + 1 podlet	1 podlet in parallel with 20R6–5
2 = CS6# (J322 in 1–2 position)	6 pF	
2 = REFRESH# (J322 in 2–3 position)	20 pF + 1 podlet	1 podlet in parallel with 20R6–5
112 = TXD1 (J325 in 1–2 position)	6 pF	
112 = DACK1# (J325 in 2–3 position)	26 pF + 1 podlet	1 podlet in parallel with 20R6–5
107 = P1.5 (J330 in 1–2 position)	6 pF	
107 = LOCK# (J330 in 2–3 position)	18 pF + 1 podlet	1 podlet in parallel with 20R6–5
INT7:0	6 pF	
TRST#, TDI, TDO, TMS, TCK[2]	6 pF	

1 The AC Loading value includes run capacitance and the input capacitance of the listed ICs.

2 This signal on connector J724 will not usually have anything connected to it.

Table 3–3: Environmental specification[3]

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)[4]
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

3 Designed to meet Tektronix standard 062-2847-00 class 5.

4 Not to exceed i386EX microprocessor thermal considerations. Forced air cooling might be required across the CPU.

Table 3–4: Certifications and compliances

EC Compliance	There are no current European Directives that apply to this product.
Pollution Degree 2	Do not operate in environments where conductive pollutants might be present.

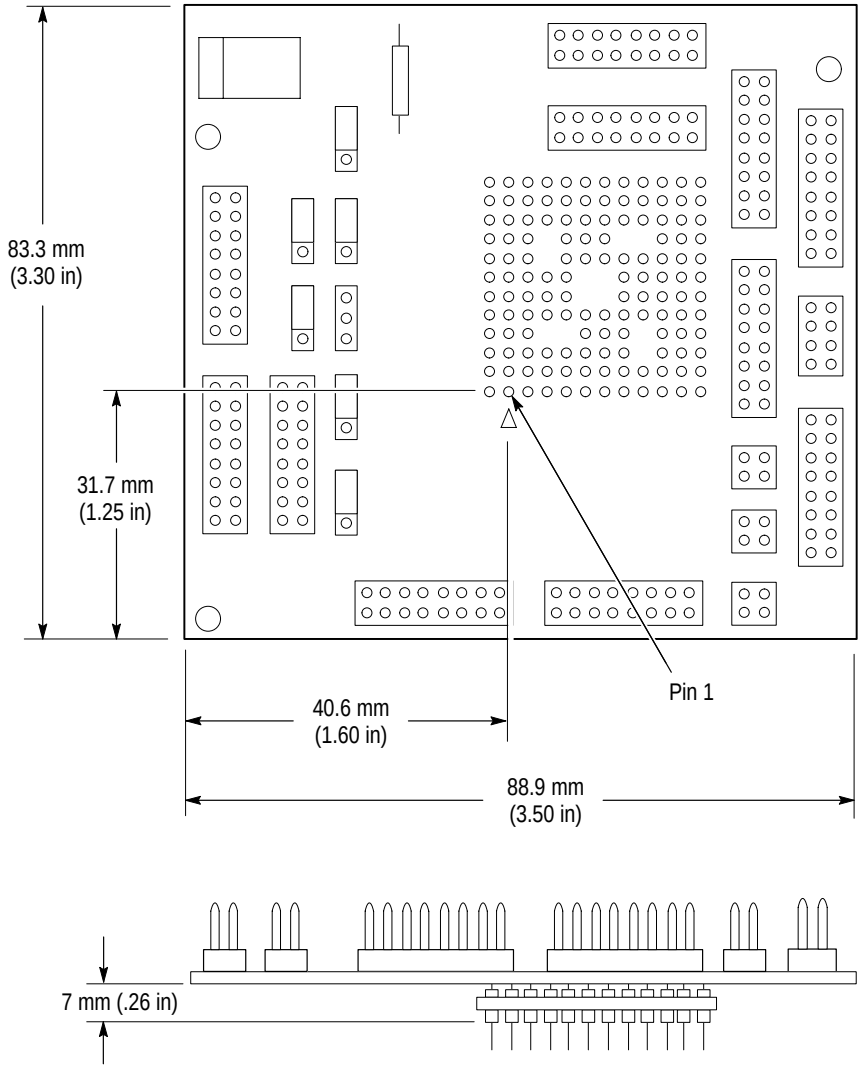


Figure 3–2: Minimum clearance of the probe adapter

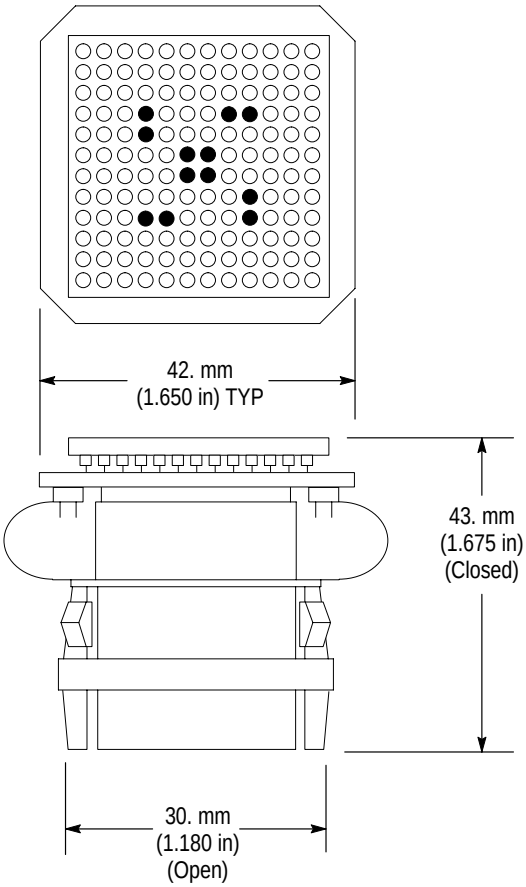


Figure 3–3: Dimensions of the test clip

Channel Assignments

Channel assignments shown in Table 3–5 through Table 3–12 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for the 102/136-channel module unless otherwise noted.
- A number sign (#) following a signal name indicates an active low signal.

Table 3–5 lists the probe section and channel assignments for the Address group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–5: Address group channel assignments

Bit order	Section:channel	i386EX signal name
25	A3:1	A25
24	A3:0	A24
23	A2:7	A23
22	A2:6	A22
21	A2:5	A21
20	A2:4	A20
19	A2:3	A19
18	A2:2	A18
17	A2:1	A17
16	A2:0	A16
15	A1:7	A15
14	A1:6	A14
13	A1:5	A13
12	A1:4	A12
11	A1:3	A11
10	A1:2	A10
9	A1:1	A9
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2
1	A0:1	A1
0	A0:0	A0

Table 3–6 lists the probe section and channel assignments for the Data group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–6: Data group channel assignments

Bit order	Section:channel	i386EX signal name
15	D1:7	D15
14	D1:6	D14
13	D1:5	D13
12	D1:4	D12
11	D1:3	D11
10	D1:2	D10
9	D1:1	D9
8	D1:0	D8
7	D0:7	D7
6	D0:6	D6
5	D0:5	D5
4	D0:4	D4
3	D0:3	D3
2	D0:2	D2
1	D0:1	D1
0	D0:0	D0

Table 3–7 lists the probe section and channel assignments for the Control group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–7: Control group channel assignments

Bit order	Section:channel	i386EX signal name
13	C2:5	LBA#
12	C2:3	BS8_L#
11	D2:6	DACK1#
10	D2:5	DACK0#
9	D2:3	SMIACT#
8	D2:2	REFRESH#
7	C2:0	RESET_L
6	C2:6	BHE#

Table 3–7: Control group channel assignments (cont.)

Bit order	Section:channel	i386EX signal name
5	C3:0	HLDA
4	C2:1	READY#
3	D2:4	LOCK#
2	C3:3	M/IO#
1	C3:7	D/C#
0	C3:2	W/R#

Table 3–8 lists the probe section and channel assignments for the Intr group, and the microprocessor signal to which each channel connects. Intr group signals are not required for disassembly. By default, this channel group is not visible.

Table 3–8: Intr group channel assignments

Bit order	Section:channel	i386EX signal name
7	C1:7	INT7
6	C1:6	INT6
5	C1:5	INT5
4	C1:4	INT4
3	C1:3	INT3
2	C1:2	INT2
1	C1:1	INT1
0	C1:0	INT0

Table 3–9 lists the probe section and channel assignments for the Copr group, and the microprocessor signal to which each channel connects. Copr group signals are not required for disassembly. Intr group signals are not required for disassembly. By default, this channel group is not visible.

Table 3–9: Copr group channel assignments

Bit order	Section:channel	i386EX signal name
2	A3:5	BUSY#
1	A3:6	ERROR#
0	A3:7	PEREQ

Table 3–10 lists the probe section and channel assignments for the ChipSel group, and the microprocessor signal to which each channel connects. ChipSel group signals are not required for disassembly. By default, this channel group is not visible.

Table 3–10: ChipSel group channel assignments

Bit order	Section:channel	i386EX signal name
7	D3:7	UCS#
6	D3:6	CS6#
5	D3:5	CS5#
4	D3:4	CS4#
3	D3:3	CS3#
2	D3:2	CS2#
1	D3:1	CS1#
0	D3:0	CS0#

Table 3–11 lists the probe section and channel assignments for the Misc group, and the microprocessor signal to which each channel connects. Misc group signals are not required for disassembly. By default, this channel group is not visible.

Table 3–11: Misc group channel assignments

Bit order	Section:channel	i386EX signal name
12	D2:7	HOLD
11	C2:4	NA#
10	C2:2	ADS#
9	D2:1	DRQ1
8	D2:0	DRQ0
7	C3:5	CLK
6	A3:4	FLT#
5	A3:3	SMI#
4	A3:2	NMI
3	C2:7	BS8#
2	C3:6	POWERDWN
1	C3:1	RD#
0	C3:4	WR#

Table 3–12 lists the probe section and channel assignments for the clock channels (not part of any group), and the microprocessor signal to which each channel connects. These channels are used only to clock in data; they are not stored as acquisition data. They must be double probed if they are to be stored in the acquisition. In this table, an _D indicates a hardware-derived signal.

Table 3–12: TMS 106 clock channel assignments

Channel	Intel 386EX microprocessor signal name
CLK0	DMA_D
CLK1	NA_D#
CLK2	CLK
CLK3	PIPE_D

These channels are used only to clock in data; they are not acquired or displayed. To acquire data from any of the signals shown in Table 3–12, you must connect another channel probe to the signal, a technique called double probing. An equals sign (=) following a signal name indicates that it is already double probed.

How Data is Acquired

This part of this chapter explains how the module acquires i386EX signals using the TMS 106 support and probe adapter. This part also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra acquisition channels available for you to use for additional connections.

386EX Clocking

A special clocking program is loaded to the module every time you load the 386EX support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the i386EX bus. The module then sends all the logged-in signals to the trigger machine and to the memory of the module for storage.

In Custom clocking, the module clocking state machine (CSM) generates one master sample for each microprocessor bus cycle, no matter how many clock cycles are contained in the bus cycle.

Figure 3–4 shows the sample points and the master sample point.

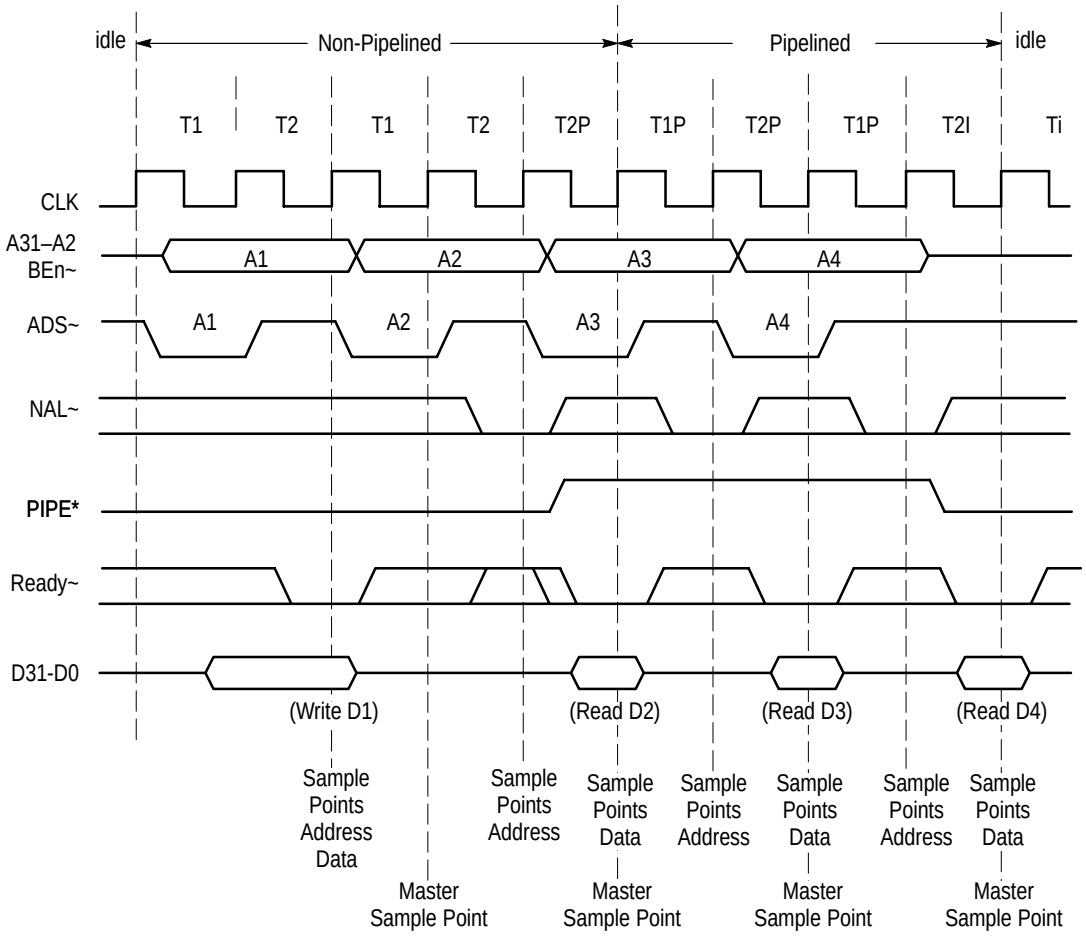


Figure 3–4: i386 EX Microprocessor Bus Timing

DMA Cycles

A DMA cycle is defined as any bus cycle initiated under the control of an alternate bus master. It does not need to be a DMA controller, such as an 82380, but can be another microprocessor. It needs only to follow the basic bus protocol of the i386EX, requiring only the CLK, NA#, BS8#, ADS#, READY#, and HLDA signals. It may support bus pipelining. DMA cycles are identified by the assertion of the HLDA, DACK1#, or DACK0# signals.

The DMA Cycles field has two options:

- Excluded

  Whenever HLDA is high, DACK1# is low, or DACK0# is low, no bus cycles are logged in. Only bus cycles driven by the i386EX will be logged in. Float cycles (cycles occurring while the FLT# signal is asserted) are stored.

- Included

  All bus cycles are logged in, including DMA cycles and backoff cycles.

Alternate Microprocessor Connections

You can connect to microprocessor signals that are not required by the support so you can do more advanced timing analysis. These signals might or might not be accessible on the probe adapter board. The following paragraphs and tables list signals that are or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–6.

Signals On the Probe Adapter

The probe adapter board contains pins for microprocessor signals that are not acquired by the TMS 106 software. You can connect extra podlets to these pins, because they can be useful for general purpose analysis. However, these signals are not defined in the Channel setup menu; you must enter the Channel setup menu and assign those signals to a new channel group.

Table 3–13 lists the microprocessor signals available on jumper J724 of the probe adapter.

Table 3–13: Signals on J724

Pin number	Signal name
1	GND
2	TRST#
3	TCK
4	TDO
5	GND
6	TDI
7	GND
8	TMS

Jumper J1530 has 132 pins, one for each pin on the i386EX PQFP package. All the microprocessor signals can be accessed by probing that signal's pin on J1530. Figure 3–5 shows the PQFP pin assignment for J1530 as viewed from the top of the board.

99	98	96	93	90	85	80	75	72	69	67	66
100	97	95	92	89	84	79	74	71	68	64	65
102	101	94	91	88	83	78	73	70	61	62	63
105	104	103	*	87	82	77	*	*	58	59	60
108	107	106	*	86	81	76	53	54	55	56	57
113	112	111	110	109	*	*	48	49	50	51	52
118	117	116	115	114	*	*	43	44	45	46	47
123	122	121	120	119	10	15	20	*	40	41	42
126	125	124	*	*	11	16	21	*	37	38	39
129	128	127	4	7	12	17	22	25	28	35	36
131	130	2	5	8	13	18	23	26	29	31	34
132	1	3	6	9	14	19	24	27	30	32	33

*** Indicates there is no connection.**

Figure 3–5: Pin Assignment for J1530

Table 3–14 lists those J1530 pins with assigned signal names.

Table 3–14: Signal names for J1530

Pin number	Signal name
74	P3.0/TMROUT0
75	P3.1/TMROUT1
77	DTR1#/SRXCLK
78	RI1#/SSIORX
79	RTS1#/SSIOTX
87	P3.7/COMCLK
98	DSR1#/STXCLK
101	P1.0/DCD0#
102	P1.1/RTS0#
104	P1.2/DTR0#
105	P1.3/DSR0#
106	P1.4/RI0#
113	EOP#/CTS1#
114	WDTOUT
129	P2.5/RXD0
131	P2.6/TXD0
132	P2.7/CTS0#

Extra Channels

Table 3–15 lists extra channels that are left after you have connected all the channels used by the disassembler. You can use these extra channels to make alternate SUT connections, and they will be logged in at the same time data is valid (READY# asserted). You can also disconnect channels not required for disassembly to make alternate connections. The channel assignment tables in this section indicate channels not required for disassembly.

Channels not defined in a channel group by the TMS 106 software are logged in with the Master sample point.

Table 3–15: Extra module sections and channels

Module	Section: channels
102-channels	Qual:1, Qual:0
136-channels	E3:7-0, E2:7-0, E1:7-0, E0:7-0, Qual:3-0
96-channels	None

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

This section contains the probe adapter discription, and information on replacing the fuse.

Probe Adapter Circuit Description

The 20R6-5 PAL takes the clock (CLK2) and divides it in half. Timing specifications for i386EX output signals do not allow using CLK2 as the logic analyzer clock due to CSM metastable conditions. This PAL produces a divided by two clock that is synchronized with the microprocessor's clock to ensure setup and to hold margins for the qualifier channels.

The 20R6-5 PAL is also used to synchronize some of the asynchronous inputs, and bring them into time alignment with all of the other signals, so that a single edge of the clock is sufficient for all.

The purpose of the 22V10C-10 is to synthesize a signal called PIPE_D, which is used as a clock qualifier. PIPE_D provides an indication to the Clocking State Machine of when the i386EX is in pipelined bus mode. The correct times for sampling the address vary as a function of pipelined operation, which can dynamically change, and is not obvious.

Replacing Signal Leads

Information on basic operations describes how to replace signal leads (individual channel and clock probes).

Replacing Protective Sockets

Information on basic operations describes how to replace protective sockets.

Replacing the Fuse

If the fuse on the i386EX probe adapter opens (burns out), you can replace it with a 1.5 A, 125 V fuse. Figure 4–1 shows the location of the fuse on the probe adapter.

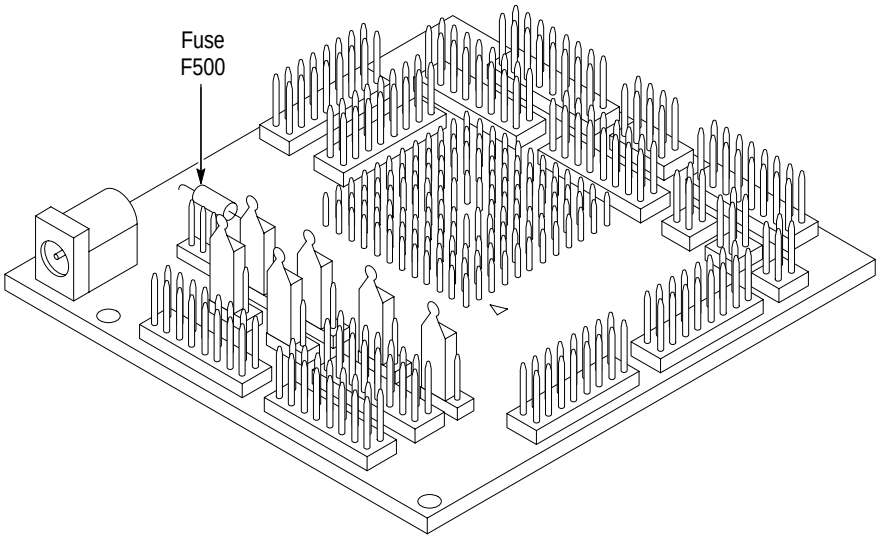


Figure 4–1: Fuse Location

Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 106 i386EX microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

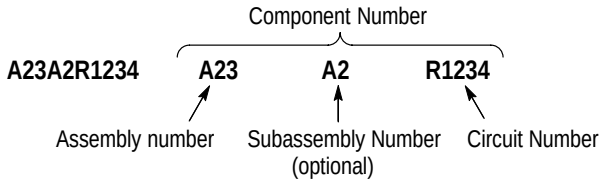
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK0875	MATSUO ELECTRONICS INC	831 S DOUBLAS ST	EL SEGUNDO CA 92641
0HHL8	EMULATION TECHNOLOGY INC	2344 WALSH AVE, BLDG F	SANTA CLARA, CA 95051
0LXM2	LZR ELECTRONICS INC	8051 CESSNA AVENUE	GAITHERSBURG MD 20879
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
04222	AVX/KYOCERA DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
50139	ALLEN–BRADLEY CO ELECTRONIC COMPONENTS	1414 ALLEN BRADLEY DR	EL PASO TX 79936
50434	HEWLETT–PACKARD CO OPTOELECTRONICS DIV	370 W TRIMBLE RD	SAN JOSE CA 95131–1008
53387	3M COMPANY ELECTRONIC PRODUCTS DIV	3M AUSTIN CENTER	AUSTIN TX 78769–2963
63058	MCKENZIE TECHNOLOGY	910 PAGE AVENUE	FREMONT CA 94538
75915	LITTELFUSE TRACOR INC SUB OF TRACOR INC	800 E NORTHWEST HWY	DES PLAINES IL 60016–3049
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01	671–3392–00			CKT BD ASSY:80386EX,QFP132 SOLDERED	80009	671339200
–	103–0417–00			ADAPTER: PQFP–132, TEST CLIP, WITH PGA SOCKET, 12 X 12 GRID	0HHL8	AC–PGA7–QF03–386–TEK
A01C340	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C421	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C515	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C540	290–5005–00			CAP,FXD,TANT:;47UF,10%,10V,5.8MM X 4.6MM	TK0875	267M–1002–476–K
A01C618	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C650	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C710	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01CR420	152–5045–00			DIODE,SIG:SCHTKY,;20V,1.2PF,24 OHM	50434	HSMS–2810–T31
A01CR440	152–5045–00			DIODE,SIG:SCHTKY,;20V,1.2PF,24 OHM	50434	HSMS–2810–T31
A01CR520	152–5045–00			DIODE,SIG:SCHTKY,;20V,1.2PF,24 OHM	50434	HSMS–2810–T31
A01F500	159–0159–00			FUSE,WIRE LEAD:1.5A,125V,5 SEC,	75915	25101.5
A01J120	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J130	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J150	131–5527–00			JACK,POWER DC:PCB,;MALE,RTANG,2MM PIN,11MMH(0.433) X 3.5MM(0.137) TAIL,9MM(0.354) W,TIN,W/SWITCH,DC PWR JACK, 2.0 MM	0LXM2	DJ005A
A01J220	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J225	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30GOLD,BD RETENTION	00779	104344–1
A01J230	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30GOLD,BD RETENTION	00779	104344–1
A01J320	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30GOLD,BD RETENTION	00779	104344–1
A01J322	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30GOLD,BD RETENTION	00779	104344–1
A01J325	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30GOLD,BD RETENTION	00779	104344–1
A01J330	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30GOLD,BD RETENTION	00779	104344–1
A01J340	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30GOLD,BD RETENTION	00779	104344–1
A01J410	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J510	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J540	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J550	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J610	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J615	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J620	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J624	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01J630	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J720	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J724	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J730	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1530	103–0324–00			ADAPTER,CONN:132 PIN MALE,PGA	63058	PGA–132M8865–12
A01R422	321–5026–00			RES,FXD:THICK FILM;4.75K OHM,1%,0.125W,TC=100 PPM	50139	BCK4751FT
A01U420	163–0238–00			IC,DIGITAL:STTL,PLD;20R6,125MHZ,20R6–5,PRGM	80009	163–0238–00
A01U515	160–8854–00			IC,DIGITAL:CMOS,PLD;PAL,22V10,10NS,180MA,386 DX 'TRACKING'	80009	160–8854–00

Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 106 i386EX microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
0HHL8	EMULATION TECHNOLOGY INC	2344 WALSH AVE, BLDG F	SANTA CLARA, CA 95051
0B445	ELECTRI–CORD MFG CO INC	312 EAST MAIN ST	WESTFIELD PA 16950
0LXM2	LZR ELECTRONICS INC	8051 CESSNA AVENUE	GAITHERSBURG MD 20879
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
14310	AULT INC	7300 BOONE AVENUE NORTH	MINNEAPOLIS MN 55428
26742	METHODE ELECTRONICS INC	7447 W WILSON AVE	CHICAGO IL 60656–4548
53387	3M COMPANY ELECTRONIC PRODUCTS DIV	3M AUSTIN CENTER	AUSTIN TX 78769–2963
63058	MCKENZIE TECHNOLOGY	910 PAGE AVENUE	FREMONT CA 94538
75915	LITTELFUSE TRACOR INC SUB OF TRACOR INC	800 E NORTHWEST HWY	DES PLAINES IL 60016–3049
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
6-1	010–0580–01			1	PROBE, ADAPTER: 80386EX, QFP–132 SOLDERED, PROBE ADAPTER	80009	010058001
6-1–1	159–0159–00			1	FUSE, WIRE LEAD: 1.5A, 125V, 5 SEC, (SEE REPL F500)		
6-1–2	131–4356–00			7	CONN, SHUNT: SHUNT/SHORTING, FEMALE, 1 X 2, 0.1 CTR, 0.63 H, BLK, WITH HANDLE, JUMPER (P225, P230, P320, P322, P325, P330, P340)	26742	9618–302–50
6-1–3	131–4530–00			7	CONN, HDR: PCB, MALE, STR, 1 X 3, 0.1 CTR, 0.230 MLG X 0.120 TAIL, 30 GOLD, BD RETENTION (SEE REPL J225, J230, J320, J322, J325, J330, J340)		
6-1–4	131–5267–00			3	CONN, HDR: PCB, MALE, STR, 2 X 40, 0.1 CTR, 0.235MLG X 0.110 TAIL, 30GOLD (SEE REPL J120, J130, J550, J410, J510, J540, J550, J610, J615, J620, J624, J630, J720, J724, J730)		
6-1–5	671–3392–00			1	CKT BD ASSY:80386EX,QFP132 SOLDERED	80009	671339200
6-1–6	131–5527–00			1	JACK, POWER DC: PCB, MALE, RTANG, 2MM PIN,11 MMH (0.433) X 3.5MM (0.137) TAIL, 9MM (0.354) W, TIN, WITH SWITCH, DC PWR JACK, 2.0 MM (J150)	80009	131–5527–00
6-2–1	103–0417–00			1	ADAPTER: TEST CLIP, PQFP–132, TEST CLIP, WITH PGA SOCKET, 12 X 12 GRID	0HHL8	AC–PGA7–QF03–386–TEK
					STANDARD ACCESSORIES		
	070–9809–01			1	MANUAL, TECH: INSTRUCTION, i386EX, DISSASEMBLER, TMS 106	80009	070–9809–01
	070–9803–00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
	119–5061–01			1	POWER SUPPLY :25W, 5V 5A, CONCENTRIC 2MM, 90–265V, 47–63HZ (NOT SHOWN)	14310	SW106KA002F01
	161–0104–00			1	CA ASSY, PWR: 3,18 AWG, 98 L, 250V/10AMP, 98 INCH, RTANG, IEC320, RCPT X STR, NEMA 15–5P, W/CORD GRIP	S3109	ORDER BY DESCRIPTION
					OPTIONAL ACCESSORIES		
	070–9802–00			1	MANUAL, TECH:BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070–9802–00
	161–0104–06			1	CA ASSY, PWR: 3, 1.0MM SQ, 250V/10AMP, 2.5 METER, RTANG, IEC320, RCPT, EUROPEAN, SAFETY CONTROLLED (OPT A1)	S3109	ORDER BY DESCRIPTION
	161–0104–07			1	CA ASSY, PWR:3, 1.0MM SQ, 240V/10AMP, 2.5 METER, RTANG, IEC320, RCPT X 13A, FUSED, UK PLUG, (13A FUSE), UNITED KINGDOM, SAFETY CONTROL (OPT A2)	S3109	ORDER BY DESCRIPTION
	161–0104–05			1	CA ASSY, PWR:3, 1.0MM SQ, 250V/10AMP, 2.5 METER, RTANG, IEC320, RCPT, AUSTRALIA, SAFETY CONTROLLED (OPT A3)	S3109	ORDER BY DESCRIPTION
	161–0167–00			1	CA ASSY, PWR:3, 0.75MM SQ, 250V/10AMP, 2.5 METER, RTANG, IEC320, RCPT, SWISS, NO CORD GRIP, SAFETY CONTROLLED (OPT A5)	S3109	ORDER BY DESCRIPTION

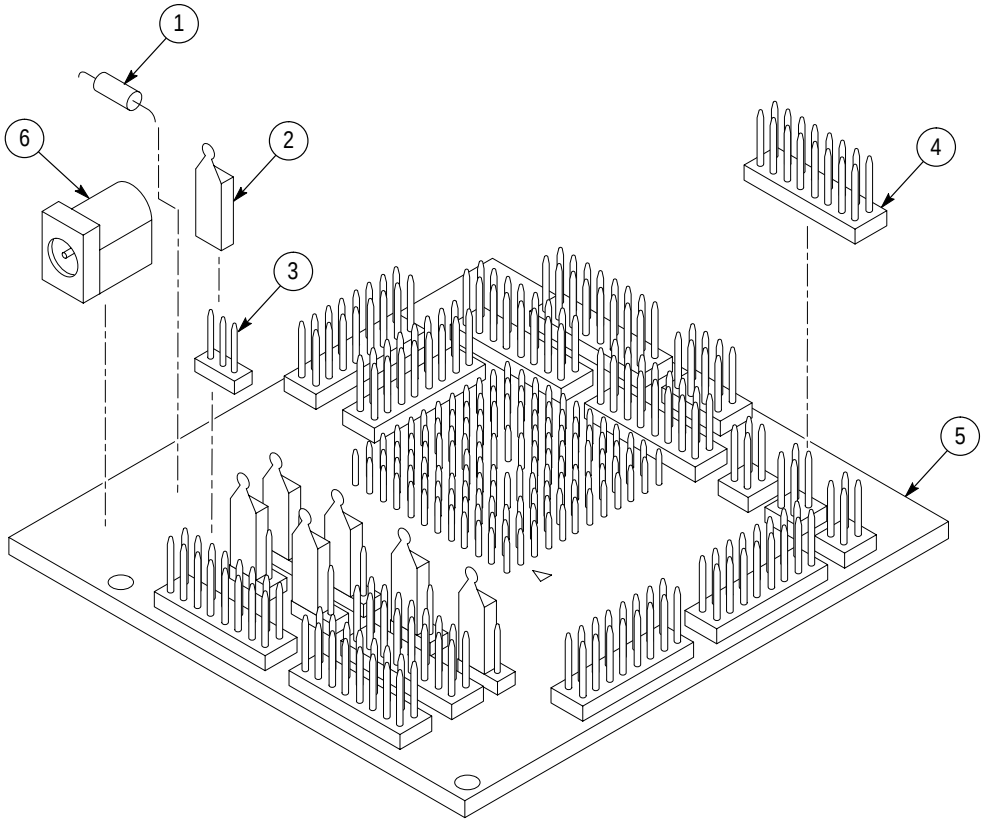


Figure 6–1: i386EX PQFP probe adapter exploded view

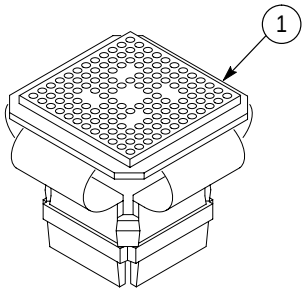


Figure 6–2: PQFP–132 Test clip with PGA socket

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